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Method for Finishing Silicon on Insulator Substrates

BACKGROUND

[0001] The present invention relates generally to an improved finishing process for manufacturing semiconductor-on-insulator (SOI) substrates, more particularly for removing damaged surface portions of semiconductor films on SOI substrates produce using an ion implantation film transfer process.

[0002] To date, the semiconductor material most commonly used in semiconductor-on-insulator structures has been single crystalline silicon. Such structures have been referred to in the literature as silicon-on-insulator structures and the abbreviation "SOI" has been applied to such structures. Silicon-on-insulator technology is becoming increasingly important for high performance thin film transistors, solar cells, and displays. Silicon-on-insulator wafers consist of a thin layer of substantially single crystal silicon 0.01-1 microns in thickness on an insulating material. As used herein, SOI shall be construed more broadly to include a thin layer of material on insulating semiconductor materials other than and including silicon.

[0003] Various ways of obtaining SOI structures include epitaxial growth of silicon on lattice matched substrates. An alternative process includes the bonding of a single crystal silicon wafer to another silicon wafer on which an oxide layer of SiO2 has been grown, followed by polishing or etching of the top wafer down to, for example, a 0.05 to 0.3 micron layer of single crystal silicon. Further methods include ion-implantation film transfer methods in which hydrogen ions are implanted in a donor silicon wafer to create a weakened layer in the wafer for separation (exfoliation) of a thin silicon layer that is bonded to another silicon wafer with an insulating (or barrier) oxide layer in between. The latter method involving hydrogen ion implantation is currently considered advantageous over the former methods.

[0004] US Patent 5,374,564 discloses a “Smart Cut” hydrogen ion implantation film transfer and thermal bonding process for producing SOI substrates. Thin film exfoliation and transfer by the hydrogen ion implantation method typically consists of the following steps. A thermal oxide film is grown on a single crystal silicon wafer (the donor wafer). The thermal
oxide film becomes a buried insulator or barrier layer between the insulator/support wafer and the single crystal film layer in the resulting of SOI structure. Hydrogen ions are then implanted into the donor wafer to generate subsurface flaws. Helium ions may also be co-implanted with the Hydrogen ions. The implantation energy determines the depth at which the flaws are generated and the dosage determines flaw density at this depth. The donor wafer is then placed into contact with another silicon support wafer (the insulating support, receiver or handle substrate or wafer) at room temperature to form a tentative bond between the donor wafer and the support wafer. The wafers are then heat-treated to about 600° C to cause growth of the subsurface flaws resulting in separation of a thin layer or film of silicon from the donor wafer. The assembly is then heated to a temperature above 1000° C to fully bond the silicon to the support wafer. This process forms an SOI structure with a thin film of silicon bonded to a silicon support wafer with an oxide insulator or barrier layer in between the film of silicon and the support wafer.

[0005] As described in US Patent 7,176,528, the ion implantation film separation technique has been applied more recently to SOI structures wherein the support substrate is a glass or glass ceramic sheet rather than another silicon wafer. This kind of structure is further referred to as silicon-on-glass (SiOG), although semiconductor materials other than silicon may be employed to form a semiconductor-on-glass (SOG) structure. Glass provides cheaper handle substrate than silicon. Also, due to the transparent nature of the glass, the applications for SOI can be expanded to areas such as displays, image detectors, thermoelectric devices, photovoltaic devices, solar cell, photonic devices, etc.

[0006] The thin layer of semiconductor material (e.g., silicon) can be amorphous, polycrystalline, or of the single crystalline type. The amorphous and polycrystalline types of devices are less expensive than their single crystal counterparts, but they also exhibit lower electrical performance characteristics. The manufacturing processes for making SOI structures with amorphous or polycrystalline layers are mature, and the performance of final products employing them is limited by the properties of the semiconductor material. In contrast to the amorphous and polycrystalline semiconductor materials, which are low quality semiconductors, single crystalline semiconductor material (such as silicon) is considered of relatively higher quality. Thus, the use of higher quality semiconductor materials will enable the manufacture of better final devices.
[0007] In an ion implantation thin film transfer fabrication process for fabricating SOI and SOG substrates, a semiconductor film or layer is exfoliated from a semiconductor donor wafer and bonded to onto an insulating support substrate, such as silicon wager or glass sheet. The surface of the exfoliated or “as-transferred” semiconductor film is not perfectly smooth. The as-transferred film typically has a surface roughness of about 10 nm. Moreover, the top portion of the as-transferred film, for example, tens of nm deep into the as transferred film, has a large degree of crystal structure damage. This damage is a result of high dose ion implantation that is required to enable the film transfer process and the heat induced exfoliation process. During implantation, the ion species (e.g., hydrogen ions, or hydrogen and helium ions) are accelerated into the semiconductor crystal lattice. While moving through the crystal lattice, the ions displace semiconductor atoms from their regular locations in the lattice. The displaced semiconductor atoms are thus disruptions or damage in a properly ordered lattice, i.e., they are defects in or damage to the overall single crystalline media. Implanted ions eventually lose their kinetic energy and come to rest in the lattice. These ions are also defects in the crystal lattice, as they are not semiconductor atoms and they are not located in proper lattice locations. Therefore, after ion implantation, the donor silicon substrate will have hydrogen contaminated and displaced semiconductor atom damaged crystal regions within and around a range of depths. Following exfoliation of the silicon exfoliation layer, a portion of this contaminated and damaged region remains on the as transferred semiconductor film or layer. As a result, the surface of the as transferred semiconductor film exhibits excessive surface roughness, ion contamination and crystal damage. The surface roughness and crystal damage detrimentally effects the fabrication and performance of electrical device formed on or in the as transferred layer. Therefore, the rough and damage portion of the surface of the as-transferred semiconductor layer or film must be removed and the surface must be smoothened.

[0008] There are several known surface removal and smoothing methods. Mechanical removal of damaged silicon is described in U.S. Patent No. 3,841,031. The polishing process involves holding and rotating a thin flat wafer of semiconductor material against a polishing surface under controlled pressure and temperature. When polishing a relatively thin transferred semiconductor film on a relatively thick substrate, however, the polishing action degrades the thickness uniformity of the transferred film. Glass surface variations are in
orders of microns, while the film to be smoothed is only fraction of a micron thick. Due to the
glass surface variations, some areas of the transferred film may get polished off completely
with typical mechanical polishing processes, forming holes in the film, while other areas of
the film may not be polished at all. Chemical-mechanical polishing (CMP) may be employed
for SOI substrates, but is very slow and expensive and may likewise form holes in the film. A
modified CMP method for smoothing silicon-on-glass uses a small computer-controlled
polishing head, as it is described, for example, in US Pat. 7,312,154, in order to uniformly thin
the film over high and low spots on the glass. This method is not advantageous, as it has a
low throughput and volume manufacturing is not possible with this method.

[0009] Removal of the damaged portion of silicon film can also be performed by etching,
either wet or dry. For wet etch of silicon, KOH can be used. For dry etch of silicon processing
in CF4 plasma can be used. However, even though the etching techniques provide removal of
the damaged silicon, they typically provide a conformal removal, so the surface of the etched
silicon film remains rough and no smoothening effect achieved. The conformal removal is due
to anisotropic etching in both, wet alkaline, and dry reactive ion etching.

[0010] Isotropic etching of silicon would provide both, damaged material removal, and
surface smoothening. Isotropic etching of silicon can be performed in, for example, so-called
HNA solution, which is a mixture of hydrofluoric, nitric, and acetic acids. However, the
HNA is highly dangerous and toxic, and therefore it does not fit well to large scale
manufacturing. Also, a nitric oxide (laughing gas) is a byproduct of silicon etching in the
HNA. The nitric oxide is highly aggressive and toxic, which make it not well suitable for the
large scale manufacturing.

[0011] Also, in silicon-on-insulator (SOI) technology, the oxidation/strip cycles are used to
obtain SOI wafers with a very thin top silicon film, much thinner than the as-transferred
silicon film. In SOI, thermal oxidation is used. The thermal oxidation is a process requiring
temperatures 900° C or higher. This cannot be used for SiOG, as most glasses can only
withstand temperatures up to about 600° C.

[0012] Further steps in the process of fabricating the SOI, such as bonding, exfoliation,
annealing and/or polishing may result in partial or total removal of implantation-induced
crystal damage. Bonding and exfoliation steps are usually performed at elevated
temperatures, which drive hydrogen ions out of the lattice due to diffusion. To completely heal the implant-induced damaged by heating (e.g., annealing), the crystal has to be heated to a temperature approaching the melting temperature of the crystal semiconductor material. For silicon, the melting temperature is 1412 °C, and heating to about 1100° C is required to almost completely heal the post-implantation crystal damage. During the process of fabricating a silicon-on-glass device, annealing to temperatures above about 600° C is prohibited because the glass warps or even melts at such high temperatures.

[0013] Another problem with the mechanical polishing processes is that they exhibit particularly poor results when rectangular SOI structures (e.g., those having sharp corners) are polished. Indeed, the aforementioned surface non-uniformities are amplified at the corners of the SOI structure compared with those at the center thereof. Still further, when large SOI structures are contemplated (e.g., for photovoltaic applications), the resulting rectangular SOI structures are too large for typical polishing equipment (which are usually designed for the 300 mm standard wafer size). Cost is also an important consideration for commercial applications of SOI structures. The polishing process, however, is costly both in terms of time and money. The cost problem may be significantly exacerbated if non-conventional polishing machines are required to accommodate large SOI structure sizes.

[0014] Melting and re-crystallization of the exfoliated semiconductor layer using excimer laser annealing is described in international publication WO/2007/142911. The excimer laser beam melts a top portion of the semiconductor layer while maintaining the glass substrate at a cooler temperature. This method results in poorer electrical characteristics within the annealed semiconductor material because the melted part of the single crystalline material solidifies too fast. In a regular Czochralski method of silicon growth, the rate of growth is around 1 millimeter per minute. In contrast, the re-growth rate of silicon melted and re-crystallized via an excimer laser is about 10E14 times faster. The relatively slow growth rate of the Czochralski method allows a nearly ideal crystal lattice to grow. At faster growth rates, there is not enough time for individual silicon atoms to diffuse to proper positions. Many silicon atoms are thus frozen at irregular locations, which means that they are structural defects in the newly formed lattice.
[0015] In commonly owned U.S. Patent Application Serial No. 12/391,340 filed on February 42, 1009, entitled Semiconductor on Insulator Made Using Improved Defect healing Process, the damaged, single crystalline silicon layer of a silicon-on-glass structure is implanted with silicon in a dose sufficient to amorphize the silicon material. The energy of the implantation is in a range sufficient to amorphize an upper, damaged portion of the single crystalline silicon, but not sufficient to amorphize the entire silicon layer. The pre-implanted substrates are then annealed at a temperature in a range between about 550 °C and 650 °C to transform the amorphous layer into a single crystalline layer. The lower, non-amorphized portion of the silicon layer serves as a seed for solid phase epitaxial re-growth.

[0016] For polysilicon annealing, the excimer laser technique is effective, as the polysilicon can be approximated as a crystal with a very high level of structural defects. In an SOI obtained by exfoliation of a single crystal semiconductor layer, however, the initial number of defects of the semiconductor material is not as high as in polysilicon. While the excimer laser annealing technique may heal some or all of the initial defects in the semiconductor material, it introduces new defects in about the same concentration as before the annealing, or even higher. Thus, the excimer laser annealing technique results in only a marginal improvement in the electrical properties of the exfoliated semiconductor layer.

[0017] An additional problem with laser annealing is that the melted semiconductor material, such as silicon, is significantly denser than crystalline silicon (2.33 and 2.57 g/cm3 respectively). When the melted silicon solidifies after the excimer laser scan, the difference between the respective densities results in a characteristic, periodic fluctuation in the thickness of the re-melted silicon. Thus, the excimer laser annealed films are inherently non-smooth, which is a disadvantage.

[0018] For the reasons discussed above, none of the aforementioned techniques and processes for removing or otherwise correcting for damage to the semiconductor lattice structure has been satisfactory in the context of manufacturing SOG structures. Thus, there is a need in the art for an improved and economical process for finishing SOI structures, and in particular SOG structures, in order to remove the damaged portion in the surface of the as transferred semiconductor layer created during ion implantation and smoothen the surface of the as transferred semiconductor layer.
SUMMARY

[0019] One or more features disclosed herein describe removal of the ion implant damaged surface portion or layer of the exfoliated semiconductor layer. The damaged layer is removed in a manner that will not degrade, or otherwise damage a glass substrate supporting the semiconductor layer. In accordance with one or more embodiments disclosed herein, methods of forming a semiconductor on glass structure, include: subjecting the as-transferred semiconductor film to an oxygen plasma treatment to oxidize the ion implant damaged layer, region or portion of the exfoliated semiconductor layer; and then stripping the oxidized layer in a wet bath, such as with a hydrofluoric acid solution, thereby removing the damaged portion of the as transferred exfoliated semiconductor layer.

[0020] According to an embodiment hereof, the method of forming a semiconductor on glass structure may include the steps of: subjecting an implantation surface of a donor semiconductor wafer to an ion implantation process to create an exfoliation layer of the donor semiconductor wafer; bonding the implantation surface of the exfoliation layer to a glass substrate; separating the exfoliation layer from the donor semiconductor wafer, thereby exposing an ion implantation damaged layer on the exfoliation layer; subjecting the at least one cleaved and damaged surface to oxygen plasma to oxidize the damaged surface layer on the exfoliation layer and convert the damaged layer to an oxide layer; and stripping the oxide layer, thereby removing the damaged layer.

[0021] The exfoliation layer may be oxidized and stripped to a depth sufficient to thin the exfoliation layer substantially to a desired final or finished thickness.

[0022] The oxygen plasma processing parameters may be in a range sufficient to oxidize an upper portion of exfoliation layer closest to the at least one cleaved surface, while not oxidizing a lower portion of the semiconductor material farther from the at least one cleaved surface.

[0023] The oxygen plasma treatment may be conducted in a plasma generated at a frequency of 1 MHz or lower, from 1 MHz to 1 kHz, or about 30 kHz or lower.

[0024] The step of bonding may include the steps of: heating at least one of the glass substrate and the donor semiconductor wafer; bringing the glass substrate into direct or indirect contact with the donor semiconductor wafer through the exfoliation layer; and
applying a voltage potential across the glass substrate and the donor semiconductor wafer to induce the bond.

[0025] The step of bonding may include maintaining the elevated temperature and the voltage for a period of time sufficient for positive ions within the oxide glass or oxide glass-ceramic to move within the glass substrate in a direction away from the semiconductor wafer, such that the glass substrate includes (i) a first glass layer adjacent to the exfoliation layer in which substantially no modifier positive ions are present, and (ii) a second glass layer adjacent the first glass layer having an enhanced concentration of modifier positive ions.

[0026] The donor semiconductor wafer may be formed of silicon (Si), germanium-doped silicon (SiGe), silicon carbide (SiC), germanium (Ge), gallium arsenide (GaAs), GaP, or InP.

[0027] According to other embodiments hereof, a method of forming a semiconductor on glass structure, may include the steps of: bonding a surface of a donor semiconductor structure to a glass substrate using electrolysis; separating a semiconductor layer, bonded to the glass substrate, from the donor semiconductor structure by exfoliation, thereby exposing at least one damaged surface on the separated semiconductor layer, the damaged surface including damage to a first depth below the damaged surface; subjecting the at least one damaged surface to an oxygen plasma treatment to oxidize the damaged surface to at least a second depth of the semiconductor material below the first depth; and removing the oxide layer, thereby removing the damaged layer from the semiconductor layer. The second depth may be substantially equal to a desired finished thickness of the exfoliation layer.

[0028] The separating step may include the steps of: implanting ions into a surface of a semiconductor wafer to form a weakened damaged layer in the donor wafer and defining the semiconductor layer in the semiconductor wafer between the weakened region the surface of the wafer; heating the implanted donor wafer to cause separation of the semiconductor layer from the donor semiconductor wafer, thereby exposing an ion implantation damaged layer on the semiconductor layer.

[0029] The step of bonding a surface of the donor semiconductor structure to the glass substrate may include the steps of: applying a voltage potential across the glass substrate and the semiconductor wafer; heating the semiconductor wafer to an elevated temperature; and maintaining the voltage potential and elevated temperature for a period of time sufficient for positive ions within the glass substrate to move within the glass substrate in a direction away
from the semiconductor wafer, such that the glass substrate includes (i) a first glass layer adjacent to the exfoliation layer in which substantially no modifier positive ions are present, and (ii) a second glass layer adjacent the first glass layer having an enhanced concentration of modifier positive ions.

[0030] Other aspects, features, advantages, etc. will become apparent to one skilled in the art when the description herein is taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] The accompanying drawings are included to provide a further understanding, and are incorporated in and constitute a part of this specification. The drawings illustrate one or more embodiment(s), and together with the description serve to explain principles and operation of the various embodiments.

[0032] Figure 1 is a diagrammatic side view of an SOG substrate fabricated using a conventional ion implantation film transfer processes;

[0033] Fig. 2 is a diagrammatic side view of a semiconductor donor wafer being implanted with ions in conventional ion implantation film transfer processes;

[0034] Fig. 3 is a diagrammatic side view of an implanted semiconductor donor wafer being bonded to a glass support or handle substrate in conventional ion implantation film transfer and anodic bonding processes;

[0001] Fig. 4 is a diagrammatic side view of the remaining portion of the semiconductor donor wafer separated from the semiconductor exfoliation layer bonded to the glass substrate in conventional ion implantation film transfer processes;

[0035] Fig. 5 is a diagrammatic side view of an SOG substrate fabricated using conventional ion implantation film transfer processes;

[0036] Fig. 6 is a diagrammatic side view of the surface of the SOG substrate undergoing an oxygen plasma conversion treatment according one embodiment described herein;

[0037] Fig. 7 is the finished SOG substrate produced as described herein;

[0038] Fig. 8 is a plot showing the thickness of the converted oxidized layer in the exfoliation layer as a function of oxygen plasma treatment time;
[0039] Fig. 9 is a plot showing the thickness of the converted oxidized layer in the exfoliation layer as a function of oxygen plasma treatment pressure; and

[0040] Fig. 10 is a plot showing the thickness of the converted oxidized layer in the exfoliation layer as a function of oxygen plasma treatment power.

DETAILED DESCRIPTION

[0041] Although the features, aspects and embodiments disclosed herein may be discussed in relation to silicon-on glass (SiOG) structures and the manufacture of SiOG structures, skilled artisans will understand that this disclosure need not be and is not limited to SiOG structures. Indeed, the broadest protectable features and aspects disclosed herein are applicable to any process in which ion implantation thin film transfer techniques are employed to transfer and bond a thin film of a semiconductor material on a glass or glass-ceramic support or handle substrate to produce a semiconductor-on-glass (SOG) structure. For ease of presentation, however, the disclosure herein is primarily made in relation to the manufacture of SiOG structures. The specific references made herein to SiOG structures are to facilitate the explanation of the disclosed embodiments and are not intended to, and should not be interpreted as, limiting the scope of the claims in any way to SiOG substrates. The processes described for the fabrication of SiOG substrates are equally applicable the manufacture of other SOG substrates and to semiconductor-on-insulator (SOI) substrates where the insulator substrate is another semiconductor substrate such as a silicon wafer. The SOI, SiOG and SOG abbreviations as used herein should be viewed as referring to semiconductor-on-glass (SOG) structures and semiconductor-on-insulator (SOI) structures in general, including, but not limited to, silicon-on-glass (SiOG) structures.

[0042] With reference to the drawings, wherein like numerals indicate like elements, there is shown in FIG. 1 an SOG structure 100 in accordance with one or more embodiments disclosed herein. The SOG structure 100 may include a glass substrate 102, and a semiconductor layer 104. The SOG structure 100 has suitable uses in connection with fabricating thin film transistors (TFTs), e.g., for display applications, including organic light-emitting diode (OLED) displays and liquid crystal displays (LCDs), integrated circuits, photovoltaic devices, solar cells, thermoelectric devices, etc.
The semiconductor material of the layer 104 may be in the form of a substantially single-crystal material. The term "substantially" is used in describing the layer 104 to take account of the fact that semiconductor materials normally contain at least some internal or surface defects either inherently or purposely added, such as lattice defects or a few grain boundaries. The term substantially also reflects the fact that certain dopants may distort or otherwise affect the crystal structure of the semiconductor material.

For the purposes of discussion, it is assumed that the semiconductor layer 104 is formed from silicon. It is understood, however, that the semiconductor material may be a silicon-based semiconductor or any other type of semiconductor, such as, the III-V, II-IV, II-IV-V, etc. classes of semiconductors. Examples of these materials include: silicon (Si), germanium-doped silicon (SiGe), silicon carbide (SiC), germanium (Ge), gallium arsenide (GaAs), GaP, and InP.

By way of example only, regular round 300 mm prime grade silicon wafers may be chosen for use as donor wafers or substrates 120 for the fabrication of SiOG structures or substrates. The donor wafers may have <001> crystalline orientation and 8-12 Ohm/cm resistivity, and be Cz grown, p-type, boron doped wafers. Crystal Originated Particle (COP) free wafers may be chosen, because the COPs might obstruct the film transfer process or disturb transistor operation. Alternatively, standard 300 mm size low doped p-type with boron concentration between 10E15 cm-3 and 10E16 cm-3 wafers manufactured by MEMC, Optia type (perfect silicon + magic demuded zone) may be used. Doping type and level in the wafers may be chosen to obtain desirable threshold voltages in eventual transistors to be subsequently made on the SiOG substrates. The largest available wafer size 300 mm may be chosen, because this will allow economical SiOG mass production. 180x230 mm rectangular donor wafers or donor tiles may be cut from the initially round wafers. The donor tile edges may be processed with a grinding tool, lasers, or other known techniques, in order to profile the edges and obtain a round or chamfered profile similar to SEMI standard edge profile. Other required machining steps, such as corner chamfering or rounding and surface polishing, may also be performed. Such donor wafer substrates or tiles may also be used to fabricate rectangular SOG structures in accordance with a further embodiment hereof. Alternatively, the donor wafer may be left as round wafers and be used to transfer round semiconductor films/exfoliation layers to square or round glass or glass ceramic substrates.
The bonding surface of the donor wafers may optionally be coated with a stiffener film as it is described in contemporaneously filed, co-pending application entitled Silicon On Glass Substrate With Stiffening Layer and Process of Making the Same.

The glass substrate 102 may be formed from a glass, glass-ceramic, oxide glass or an oxide glass-ceramic. Although not required, the embodiments described herein may include an oxide glass or glass-ceramic exhibiting a strain point of less than about 1,000 degrees C. As is conventional in the glass making art, the strain point is the temperature at which the glass or glass-ceramic has a viscosity of $10^{14.6}$ poise ($10^{13.6}$ Pa.s). As between oxide glasses and oxide glass-ceramics, the glasses may have the advantage of being simpler to manufacture, thus making them more widely available and less expensive. By way of example, a glass substrate may be formed from glass containing alkaline earth ions, such as Gen 2 size substrates made of Corning Incorporated glass composition no. 1737, Corning Incorporated Eagle 2000™ glass, or Corning Incorporated Eagle XG™ glass. These Corning Incorporated fusion formed glasses have particular use in, for example, the production of liquid crystal displays. Moreover, the low surface roughness of these glasses that is required for fabrication of liquid crystal display backplanes on the glass is also advantageous for effective bonding as described herein. Eagle glass is also free from heavy metals and other impurities, such as arsenic, antimony, barium, that can adversely affect the silicon exfoliation/device layer. Being designed for the manufacture of flat panel displays with polysilicon thin film transistors, Eagle glass has a carefully adjusted coefficient of thermal expansion (CTE) that substantially matches the CTE of silicon, e.g. a Eagle glass has a CTE of $3.18 \times 10^{-6}$ C-1 at 400° C and silicon has a CTE of $3.2538 \times 10^{-6}$ at 400° C. Eagle glass also has a relatively high strain point of 666° C, which is higher than the temperature needed to trigger exfoliation (typically around 500° C). These two features, e.g. ability to survive exfoliation temperatures and CTE match with silicon, are main reasons for choosing Eagle glass for the silicon layer transfer and bonding. Since exfoliation of the donor wafer typically happens around 500° C, the strain point of the glass should be greater than 500° C.

The glass substrate 102 may have a thickness in the range of about 0.1 mm to about 10 mm, such as in the range of about 0.5 mm to about 3 mm. For some SOI structures, insulating layers having a thickness greater than or equal to about 1 micron are desirable, e.g., to avoid parasitic capacitive effects which arise when standard SOI structures having a silicon/silicon
dioxide/silicon configuration are operated at high frequencies. In the past, such thicknesses have been difficult to achieve. In accordance with the present invention, an SOI structure having an insulating layer thicker than about 1 micron is readily achieved by simply using a glass substrate 102 having a thickness that is greater than or equal to about 1 micron. A lower limit on the thickness of the glass substrate 102 may be about 1 micron. In general, the glass substrate 102 should be thick enough to support the semiconductor layer 104 through the bonding process steps, as well as subsequent processing performed on the SiOG structure 100. Although there is no theoretical upper limit on the thickness of the glass substrate 102, a thickness beyond that needed for the support function or that desired for the ultimate SOG structure 100 might not be advantageous since the greater the thickness of the glass substrate 102, the more difficult it will be to accomplish at least some of the process steps in forming the SOG structure 100.

[0049] The glass substrates may be rectangular in shape and may be large enough to hold several donor wafers arrayed on the bonding surface of the glass. In which case, a single donor wafer-glass assembly as placed into the furnace/bonder for film transfer would include a plurality of donor wafers arrayed on the surface of a single glass sheet. The donor wafers may be round semiconductor donor wafers or they may be rectangular semiconductor donor wafers/tiles. The resulting SOG product would comprise a single glass sheet with a plurality of round or rectangular silicon films bonded thereto.

[0050] Reference is now made to FIGS. 2-7, which illustrate intermediate structures that may be formed in carrying out the process of manufacturing the SOG structure 100 of FIG. 1 in accordance with one or more aspects of the present invention.

[0051] Turning first to FIG. 2, an implantation surface 121 of a donor semiconductor wafer 120 is prepared, such as by polishing, cleaning, etc. to produce a relatively flat and uniform implantation surface 121 suitable for bonding to the glass or glass-ceramic substrate 102. The bonding surface 121 of the donor wafer 120 is cleaned to remove dust and contaminants in preparation for bonding. The donor wafer may be cleaned by processing the donor wafer in an RCA solution and drying. For the purposes of discussion, the semiconductor wafer 120 may be a substantially single crystal Si wafer, although as discussed above any other suitable semiconductor conductor material may be employed.
The glass sheets 102, or other material substrates to be used as the support substrate, are also cleaned to remove dust and contaminants in preparation for bonding. The glass sheets may be cleaned and rendered hydrophilic for bonding using a wet ammonia process to remove dust and contaminants and terminate the glass surface with hydroxyl groups for rendering the bonding surface of the glass highly hydrophilic for bonding of the glass 102 to the bonding surface 121 of the donor wafer 120. The glass sheets may then be rinsed in de-ionized water and dried. One of skill in the art will understand how to formulate suitable washing solutions and procedures for the donor wafers and the glass (or other material) support substrates.

An exfoliation layer 122 is created by subjecting the implantation surface 121 to one or more ion implantation processes to create a weakened region 123 below the implantation surface 121 of the donor semiconductor wafer 120. Although the embodiments of the present invention are not limited to any particular method of forming the exfoliation layer 122, Hydrogen ions (such as H\(^+\) and/or H\(^{2+}\) ions) are implanted (as indicated by the arrows in Fig. 2) into the bonding surface 121 of the donor wafer 120 to a desired depth to form a damage/weakened zone or layer 123 in the silicon donor wafer 120. Co-implantation of Helium ions into the bonding surface 121 of the donor wafer in addition to the Hydrogen ions, as is well understood in the art, may also be employed to form the weakened region 123. An exfoliation layer 122 (with the oxide layer 146 and the barrier layer 142 thereon) is thereby defined in the donor wafer 120 between the damaged zone 123 and the bonding surface 121 of the donor wafer. As is well understood in the art, the ion implantation energy and density may be adjusted to achieve a desired thickness of the exfoliation layer 122, such as between about 300-500 nm, although any reasonable thickness may be achieved.

Appropriate implantation energies for a desired thickness of transferred film (e.g. implantation depth) can be calculated using a SRIM simulation tool. As the ion stopping powers of silicon and silicon nitride are different, the Si/ Si\(_3\)N\(_4\) target has to be modeled in the SRIM input in order to calculate the appropriate implantation energy. One of skill in the art will understand how to determine an appropriate implantation energy for a desired implantation depth for any given implantation ion or species, donor wafer material, barrier layer material, and any other material layers on the bonding surface 121 of the bonding wafer. For example, for H\(^{2+}\) ions implanted at an energy of 60 keV through a 100 nm Si\(_3\)N\(_4\) barrier
layer into the donor wafer 120 will form an exfoliation layer 122, including the Si₃N₄ barrier layer, having a thickness of about 205 nm for transfer.

[0055] Regardless of the nature of the implanted ion species, the effect of implantation on the exfoliation layer 122 is the displacement of atoms in the crystal lattice from their regular locations. When the atom in the lattice is hit by an ion, the atom is forced out of position and a primary defect, a vacancy and an interstitial atom, is created, which is called a Frenkel's pair. If the implantation is performed near room temperature, the components of the primary defect move and create many types of secondary defects, such as vacancy clusters, etc. The vacancy clusters may be annealed at temperatures exceeding 900 °C; however, as discussed above, to completely heal implant-induced damaged by annealing, the exfoliation layer 122 would have to be heated to a temperature approaching the melting temperature of the semiconductor material, which would warp or even melt the glass substrate 102 (which is added later in the manufacturing process). If annealing was carried out at a lower temperature, such as 600 °C, the exfoliation layer 122 would still contain defects, such as the aforementioned vacancy clusters and other impurity-vacancy clusters. Most of these types of defects are electrically active, and serve as traps for major carriers in the semiconductor lattice. Therefore, the concentration of free carriers in the exfoliation layer 122 is lower when post-implantation defects are present. The electrical resistivity of defect laden semiconductor material is also worsened compared to defect-free semiconductor material. A process for removing the implantation-induced defects will be discussed later in this description.

[0056] With reference now to FIG. 3, the bonding surface 121 of the exfoliation layer 122 (with the barrier layer 142 thereon) is then pre-bonded to the glass support substrate 102. The glass and the wafer, especially in the case of rectangular donor wafer or tile, may be pre-bonded by initially contacting them at one edge, thereby initiating a bonding wave at the one edge, and propagating the bonding wave across the donor wafer and support substrate to establish a void free pre-bond. Alternatively, pre-bonding may be performed by mating the glass substrates and donor tiles or wafers at desired point and applying pressure at the desired point of the contacted pair to initiate a bonding wave. The bonding wave proceeds across entire contacted surfaces in about 10 to 20 seconds. The resulting intermediate structure is thus a stack including the exfoliation layer 122 of the semiconductor donor wafer 120, a remaining portion 124 of the donor wafer 120, and the glass support substrate 102.
[0057] The glass substrate 102 may now be bonded to the exfoliation layer 122 using an electrolysis process (also referred to herein as an anodic bonding process) as illustrated in Fig. 3, or by a thermal bonding process such as a “Smart Cut” thermal bonding process. A basis for a suitable anodic bonding process may be found in U.S. Patent No. 7,176,528, the entire disclosure of which is hereby incorporated herein by reference. Portions of this process are discussed below. A basis for a suitable Smart Cut thermal bonding process, which may alternatively be employed, may be found in U.S. Patent No. 5,374,564, the entire disclosure of which is hereby incorporated herein by reference.

[0058] According to one embodiment disclosed herein, the pre-bonded glass-donor wafer assemblies are placed in a furnace/bonder for bonding and film transfer/exfoliation. The glass-donor wafer assemblies may be placed horizontally in a furnace or bonder in order to prevent the remaining portions of the donor wafers from sliding on the newly transferred exfoliation layer following exfoliation and scratching the newly created silicon film 122 on the glass substrate substrates 102. The glass-donor wafer assemblies may be arranged in the furnace with the silicon donor wafer 120 on the bottom, downward facing side of the glass support substrate 102. With this arrangement, the remaining portion 124 of the silicon wafer may be allowed to simply drop down away from the newly exfoliated and transferred exfoliation layer 122 following exfoliation or cleaving of the exfoliation layer 122. Scratching of the newly created silicon film (the exfoliation layer) on the glass may thus be prevented. Alternatively, the glass-donor wafer assemblies may be placed horizontally in the furnace with the donor wafer on top of the glass substrate. In which case, the remaining portion 124 of the donor wafer must be carefully lifted from the glass substrate to avoid scratching the newly exfoliated silicon film 122 on the glass.

[0059] Once the pre-bonded glass-silicon assembly is loaded into the furnace, the furnace may be heated to 100-200° C and maintained at that temperature for about 1 hour, for example, during a first heating step. This first heating step increases the bonding strength between the silicon and the glass thus eventually improving layer transfer yield. The temperature may then be ramped at slow rate of about 10° C per minute up to as high as 600° C to cause exfoliation during a second heating step. Ramping the temperature too quickly may result in temperature gradients that cause mechanical stresses. The stresses may cause various defects in the SiOG substrates as canyons, sheet warpage, etc. When temperature
reaches about 300 to 500° C, the exfoliation layer 122 separates or exfoliates from the remaining portion 124 of the donor semiconductor wafer 120. The result is an SOG structure 100, including a glass substrate 102 with the relatively thin exfoliation layer 122 formed of the semiconductor material of the donor semiconductor layer 120 bonded thereto. The separation may be accomplished via fracture of the exfoliation layer 122 due to thermal stresses. Alternatively or in addition, mechanical stresses such as water jet cutting or chemical etching may be used to facilitate the separation.

[0060] After exfoliation, temperature in the furnace may continue to rise until it reaches about 600° C. The newly formed SOG substrate 100 and the remaining portion of the donor wafers or tiles may optionally be annealed during 12 hours thermal treatment at 600° C in an inert atmosphere. During this annealing step the implantation-induced defects are partially annealed. It is not possible to anneal all the defects. Some of the defects are stable at temperature above 600° C, whereas Eagle glass and other glasses can only withstand temperatures up to about 600° C. The non-annealed defects are typically electrically active and adversely affect the electrical properties of the SiOG structure. Also, during this annealing step, hydrogen is completely removed from silicon donor wafer and the exfoliation layer. The Si film on SiOG substrates 100 obtained this way has electrical properties that are close to electrical properties of the bulk silicon tiles from which the film was delaminated. The furnace is cooled down, and SiOG substrates and the remaining portions of the donor leftover tiles are unloaded from the furnace.

[0061] By way of example, the temperature during the second heating step may be within about +/- 350° C of a strain point of the glass substrate 102, more particularly between about -250 °C and 0° C of the strain point, and/or between about -100° C and -50° C of the strain point. Depending on the type of glass, such temperature may be in the range of about 500-600° C. In addition to the above-discussed temperature characteristics, mechanical pressure (as indicated by the arrows 130 in Fig. 3) may be applied to the intermediate assembly. The pressure range may be between about 1 to about 50 psi. Application of higher pressures, e.g., pressures above 100 psi, might cause breakage of the glass substrate 102. One skilled in the art can properly design furnace processing for exfoliation as it is described herein and as described, for example, in U.S. Patent Nos. 7,176,528 and 5,374,564, and U.S. published patent application Nos. 2007/0246450 and 2007/0249139.
The glass substrate 102 may be heated to a higher temperature than the donor semiconductor wafer 120 and exfoliation layer 122. By way of example, the temperature difference between the glass substrate 102 and the donor semiconductor wafer 120 (and the exfoliation later 122) is at least 1 °C, although the difference may be as high as about 100 to about 150 °C. This temperature differential is desirable for a glass having a coefficient of thermal expansion (CTE) matched to that of the donor semiconductor wafer 120 (such as matched to the CTE of silicon) since it facilitates later separation of the exfoliation layer 122 from the semiconductor wafer 120 due to thermal stresses.

According to one embodiment hereof, anodic bonding may be employed. In the case of an anodic bonding, a voltage potential (as indicated by the arrows and the + and - in Fig. 3) is applied across the intermediate assembly during the second heating step. For example a positive electrode is placed in contact with the semiconductor donor wafer 120 and a negative electrode is placed in contact with the glass substrate 102. The application of a voltage potential across the stack at the elevated bonding temperature during the second heating step induces alkali, alkaline earth ions or alkali metal ions (modifier ions) in the glass substrate 102 adjacent to the donor wafer 120 to move away from the semiconductor/glass interface further into the glass substrate 102. More particularly, positive ions of the glass substrate 102, including substantially all modifier ions, migrate away from the higher voltage potential of the donor semiconductor wafer 120, forming: (1) a reduced (or relatively low as compared to the original glass 136/102) positive ion concentration layer 132 in the glass substrate 102 adjacent the exfoliation layer 122; (2) an enhanced (or relatively high as compared to the original glass 136/102) positive ion concentration layer 134 in the glass substrate 102 adjacent the reduced positive ion concentration layer; while leaving (3) a remaining portion 136 of the glass substrate 102 with an unchanged ion concentration (e.g. the ion concentration of remaining layer 136 is the same as the original “bulk glass” substrate 102). The reduced positive ion concentration layer 132 in the glass support substrate performs a barrier functionality by preventing positive ion migration from the oxide glass or oxide glass-ceramic into the exfoliation layer 122.

With reference now to FIG. 4, after the intermediate assembly is held under the conditions of temperature, pressure and voltage for a sufficient time (such as about an hour), the voltage is removed and the intermediate assembly is allowed to cool to room temperature.
The remaining portion 124 of the donor wafer 120 is removed from the exfoliation layer 122, leaving the exfoliation layer bonded to the glass substrate 102. This may include some mechanical peeling if the exfoliation layer 122 has not already become completely free from the remaining portion 124 of the donor wafer 120. The results is an SOG structure or substrate 100, e.g. a glass substrate 102 with the relatively thin exfoliation layer or film 122 of semiconductor material bonded to the glass substrate 102.

[0065] As illustrated in Fig. 5, after separation of the exfoliation layer 122 from the remaining portion 124 if the donor wafer, the resulting SOG structure 100 includes the glass substrate 102 and the exfoliation layer 122 of semiconductor material bonded thereto. The cleaved or exfoliated surface 125 of the SOI structure, just after exfoliation, may exhibit excessive surface roughness, excessive silicon layer thickness and implantation damage of the silicon layer. The exfoliation layer 122 of the intermediate structure includes two basic layers 122A, 122B. A first rough, first or damaged portion or layer 122A, closest to the cleaved surface 125, includes implantation induce defects and damage resulting from the ion implantation process as previously described, which damage extend to a first damaged depth below the surface of the silicon layer. A second undamaged portion or layer 122B, below the damaged portion 122A, is substantially free from any implantation-induced defects. The highest concentration of defects within the first layer 122A is expected nearest to the cleaved surface 125.

[0066] Transmission electron microscopy (TEM) analysis of a damaged layer 122A of Si exfoliation layer 122 obtained in an ion implantation film transfer process using a single hydrogen implant at energy 30 keV reveals that the damaged layer comprises about a 70 nm thick layer of the surface portion of the exfoliation layer 122. The damage layer will be thicker if hydrogen implantation energy is higher, or thinner, if dual implant techniques like helium-then-hydrogen are employed. The surface of the as-transferred film typically has significant roughness, for example a roughness of about 10 nm RMS, as can be verified using atomic force microscopy (AFM). The surface roughness can be lower or higher then 10 nm, depending on film transfer process conditions, but it is typically undesirably high for effective further semiconductor device fabrication on the SOG structure 100.
[0067] With reference now to FIG. 6, according to an embodiment hereof, the damaged portion or layer 122A of the transferred silicon film is removed and the surface roughness of film surface is improved with an oxygen plasma treatment of the exfoliated surface 125 of the as transferred exfoliation layer 122. The oxygen plasma treatment oxidizes the near surface damaged region or layer 122A of the as transferred film 122 and converts it to a SiO$_2$ layer. The plasma processing conditions are chosen such that a thickness or depth of the oxidized SiO$_2$ layer is equal or slightly greater than the thickness of the first or damaged depth of the damaged layer 122A of the silicon film. To determine the right thickness to be oxidized, the thickness of the damaged silicon has to be measured first using an appropriate technique, for example, with a transmission electron microscope. A thickness of the damaged portion or layer on the surface of the transferred silicon film formed with co-implantation of hydrogen and helium ions typically falls into a range from 10 nm to 100 nm thick, for which there are plasma processing conditions that allow for complete oxidizing of the damaged portion of the silicon film. The plasma processing conditions may alternatively be chosen such that a thickness or depth of the oxidized SiO$_2$ layer is equal or slightly greater than a predetermined or desired final or finished thickness of the silicon film on the SOG structure or substrate, which may be greater than the thickness of the damages layer 122A.

[0068] The plasma oxidation process can be performed in a reactive ion etch (RIE) type plasma etching setup. In this type of a tool, the SOG substrate is plasma oxidized while the SOG substrate remains near-room temperature. This is beneficial for the SiOG, as there is no thermally-induced stress in the SOG substrate. Optionally, the plasma oxidation can be performed using PECVD tools. The PECVD tools have a controlled heating of the processed substrates. With the PECVD the plasma oxidation can be performed at elevated temperatures, while only heating the glass substrate up to a temperature that glass material can withstand, e.g. up to 600° C. Plasma oxidation at elevated temperature allows faster oxide growth and increased throughput.

[0069] The proper plasma conditions for oxidizing/converting the surface 125 of the exfoliation layer to the proper depth to remove the damaged layer 122A may be chosen using calibration curves similar to ones shown in Fig.8 through Fig.10. Figs. 8 through 10 show calibration curves for the thickness of the converted oxide layer in the surface of a silicon film as a function of three main plasma processing parameters, namely the power applied to the
plasma from generator, the pressure of oxygen in the plasma chamber, and the processing time in the plasma chamber. Fig. 8 is a calibration curve for the thickness in nanometers of the converted/oxidized layer obtained in the surface of an as-exfoliated silicon film as a function plasma processing time in seconds. Fig. 8 shows that the thickness in nanometers of the oxidized layer in a silicon film monotonically increases with plasma processing time. Fig.9 and Fig.10 are similar calibration curves for the thickness of the oxidized layer as a function of plasma power and for pressure in the plasma chamber, respectively. The calibration curves in Figs. 8 through 10 were obtained using a plasma tool having 30 kHz plasma generator. For plasma tools having different type of excitation, such as DC generators, 13.56 MHz generators, or microwave generators, the proper calibration curves can be easily obtained by one skilled in the art.

[0070] The finishing process in accordance with an embodiment hereof includes subjecting the cleaved surface 123 of the silicon exfoliation layer 122 to an oxygen plasma treatment process sufficient to oxidize the near surface region of the exfoliation layer to a depth at least coextensive with or below the first damaged layer 122A of the exfoliation layer 122, thereby converting at least damaged layer 122A if the semiconductor exfoliation layer 122 into a sacrificial oxide layer 122A. In the case of a Si donor wafer and exfoliation layer, at least the damaged layer 122A having a thickness in a range from about 10 nm to about 100 nm is converted into a sacrificial SiO₂ layer by contact with oxygen plasma. Thereafter, the sacrificial oxide layer, and therefore the previously damaged Si layer 122A, is stripped by bathing the SOG substrate 100 in a hydrofluoric acid (HF) or other suitable acid or etching solution as illustrated in Fig. 7. The damaged layer 122A is thus effectively removed from the surface 125 of the exfoliation layer 125. The underlying Si layer 122B acts as an etch stop for halting the removal of material at the correct depth, e.g. at the surface of the Si layer 122B.

[0071] In order to convert the damaged layer 122A into a SiO₂ sacrificial layer 148, the exfoliation surface 125 of the SOG substrate 100 may be processed in a low frequency, 30 kHz Technics plasma tool. Oxygen plasma conversion is not limited to low frequency plasma tools. RF, microwave, and other types of plasma equipment and processes can be employed as well. Through routine experimentation, one skilled in the art can select proper plasma equipment and conditions, such as plasma power, processing time, oxygen flow, and pressure in the chamber, required to convert the desired thicknesses of the Si or semiconductor
exfoliation layer into an oxide layer of a sufficient depth or thickness for removal of the entire
damaged layer 122A.

[0072] According to an embodiment thereof, in order for the oxygen plasma treatment to
oxidize and convert the damaged surface of the exfoliation to a depth of about 10 nm to about
100 nm thick, (as is require to completely remove the damaged layer) the oxygen plasma is
generated at a relatively low frequency in the kHz range. The oxygen plasma may be
generated at frequency of 1 MHz or lower, from 1 kHz to 1 MHz, or at about 30 kHz. One
skilled in the art can properly choose HF concentration in the bath and etching time. After the
oxide stripping, the SiOG substrate is cleaned and the process is complete. The processed
SiOG substrate has no damaged portion of the silicon film. Roughness of silicon film surface
is also improved. AFM analysis of the processed SiOG substrate showed that both, RMS
roughness and peak-to-valley roughness improved.

[0073] Compared to prior art techniques of addressing the implantation damage problem, the
embodiments of the present invention are less expensive to implement. For example, the prior
art polishing technique requires at least one hour per square foot of polishing time, resulting in
only a 50 nm or less material removal. In contrast, the techniques of one or more
embodiments of the present invention require a few minutes in a plasma chamber followed by
an acid strip. Therefore, the presently disclosed process is relatively straight forward.
Moreover, compared to the prior art polishing technique, the one or more methods of the
present invention result in higher quality final products. Indeed, the polishing process results
in degradation of thickness uniformity of the exfoliation layer 122, while the This advantage
is more pronounced for very thin exfoliation layers of about 100 nanometers and less.

[0074] Although the invention herein has been described with reference to particular
embodiments, it is to be understood that these embodiments are merely illustrative of the
principles and applications of the present invention. It is therefore to be understood that
numerous modifications may be made to the illustrative embodiments and that other
arrangements may be devised without departing from the spirit and scope of the present
invention as defined by the appended claims.
FIG. 3

FIG. 4
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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CLAIMS:

1. A method of forming a semiconductor on glass structure, comprising:
   - subjecting an implantation surface of a donor semiconductor wafer to an ion
     implantation process to create an exfoliation layer of the donor semiconductor wafer;
   - bonding the implantation surface of the exfoliation layer to a glass substrate;
   - separating the exfoliation layer from the donor semiconductor wafer, thereby exposing
     an ion implantation damaged layer on the exfoliation layer;
   - subjecting the damaged layer to oxygen plasma to oxidize the damaged layer on the
     exfoliation layer and convert the damaged layer to an oxide layer; and
   - stripping the oxide layer, thereby removing the damaged layer and thinning the
     exfoliation substantially to a desired end thickness.

2. The method of claim 1, wherein the oxygen plasma processing parameters are
   in a range sufficient to oxidize the damaged layer exfoliation layer, while not oxidizing an
   undamaged lower portion of the semiconductor exfoliation layer.

3. The method of claim 2, wherein a thickness undamaged lower portion of the
   semiconductor exfoliation layer is substantially equal to a desired finished thickness of the
   exfoliation layer.

4. The process of claim 3, wherein the plasma treatment is conducted in a plasma
   generated at a frequency of 1 MHz or lower.

5. The process of claim 4, wherein the plasma treatment is conducted in a plasma
   generate at a frequency of from 1 MHz to 1 kHz, or about 30 kHz or lower.

6. The method of claim 1, wherein the step of bonding includes:
   heating at least one of the glass substrate and the donor semiconductor wafer to an
   elevated temperature;
bringing the glass substrate into direct or indirect contact with the donor semiconductor wafer through the exfoliation layer; and

applying a voltage potential across the glass substrate and the donor semiconductor wafer to induce bonding.

7. The method of claim 6, wherein the step of bonding includes maintaining the elevated temperature and the voltage for a period of time sufficient for positive ions within the glass substrate to move within the glass substrate in a direction away from the semiconductor wafer, such that the glass substrate includes (i) a first glass layer adjacent to the exfoliation layer in which substantially no modifier positive ions are present, and (ii) a second glass layer adjacent the first glass layer having an enhanced concentration of modifier positive ions.

8. The method of claim 1, wherein the donor semiconductor wafer is taken from the group consisting of: silicon (Si), germanium-doped silicon (SiGe), silicon carbide (SiC), germanium (Ge), gallium arsenide (GaAs), GaP, and InP.

9. A method of forming a semiconductor on glass structure, comprising:

bonding a surface of a donor semiconductor structure to a glass substrate using electrolysis;

separating a semiconductor layer, bonded to the glass substrate, from the donor semiconductor structure by exfoliation, thereby exposing a damaged surface on the separated semiconductor layer, the damaged surface including damage to a first depth below the damaged surface;

subjecting the at least one damaged surface to an oxygen plasma treatment to oxidize the damages surface to at least a second depth of the semiconductor material of equal depth or below the first depth; and

removing the oxide layer, thereby removing the damaged layer from the semiconductor layer.
10. The method of claim 9, wherein a remaining undamaged portion of the semiconductor layer is substantially equal to a desired finished thickness of the exfoliation layer.

11. The process of claim 10, wherein the plasma treatment is conducted in a plasma generated at a frequency of 1 MHz or lower.

12. The process of claim 11, wherein the plasma treatment is conducted in a plasma generate at a frequency of from 1 MHz to 1 kHz, or about 30 kHz or lower.

13. The process of claim 9, wherein the separating step includes:
implanting ions into a surface of the donor semiconductor structure to form a weakened damaged layer in the donor semiconductor structure and defining the semiconductor layer in the donor semiconductor structure between the weakened region the surface of the wafer;
heating the implanted donor semiconductor structure to cause separation of the semiconductor layer from the donor semiconductor structure, thereby exposing an ion implantation damaged layer on the donor semiconductor structure.

14. The method of claim 9, wherein the step of bonding a surface of the donor semiconductor structure to the glass substrate includes:
applying a voltage potential across the glass substrate and the donor semiconductor structure;
heating the donor semiconductor structure and the glass substrate to an elevated temperature; and
maintaining the voltage potential and elevated temperature for a period of time sufficient for positive ions within the glass substrate to move within the glass substrate in a direction away from the semiconductor wafer, such that the glass substrate includes (i) a first glass layer adjacent to the exfoliation layer in which substantially no modifier positive ions are present, and (ii) a second glass layer adjacent the first glass layer having an enhanced concentration of modifier positive ions.
ABSTRACT

A process for removing the damaged surface portion of a semiconductor layer on a semiconductor-on-insulator structure or a semiconductor-on-glass structure is provided. The damaged surface layer is treated with an oxygen plasma to oxidize the damaged layer and convert the damaged layer into an oxide layer. The oxide layer is then stripped in a wet bath, such as hydrofluoric acid bath, thereby removing the damaged portion of the semiconductor layer. The damaged layer may be an ion implantation damaged layer resulting from an ion implantation film transfer processes used to make the semiconductor-on-insulator structure or the semiconductor-on-glass structure.
PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 C.F.R. § 1.53(c).

INVENTOR(S)

Given Name and Family Name or Surname  Residence (City and either State or Foreign Country)
Alex Usenko  22 Indian Pipe Court, Painted Post, NY 14870 USA

TITLE OF THE INVENTION (280 characters max)

METHOD FOR FINISHING SILICON ON INSULATOR SUBSTRATES

CORRESPONDENCE ADDRESS

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ENCLOSED APPLICATION PARTS (check all that apply)

☐ Specification Number of Pages: 26  ☐ Small Entity Statement
☐ Drawing(s) Number of Pages: 4  ☐ Other (specify):

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☐ No.
☐ Yes, the name of the U.S. Government agency and the Government contract number are:

Respectfully submitted,

SIGNATURE: [Signature] Date: 6/30/10

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February 2, 2009